CURRENT STATUS OF THE RAON MACHINE PROTECTION SYSTEM DEVELOPMENT

Hyunchang Jin*, Yongjun Choi, Sangil Lee
Rare Isotope Science Project, Institute for Basic Science, 34047 Daejeon, Korea

Abstract

For the RAON accelerator that transports beams with high energy and power, a machine protection system (MPS) that protects each device from sudden beam loss is necessary. For this reason, we have been preparing for the development of the MPS with the start of the RAON accelerator construction. For effective MPS operation and stable accelerator operation, we divided the MPS into four subsystems: fast protection system, slow interlock system, run permit system, and post-mortem system. Among them, the FPGA-based fast protection system and the PLC-based slow interlock system have been tested by prototypes and are currently working on the mass production. The run permit system and the post-mortem system are also undergoing basic design and software development. In this paper, we will describe the progress of the MPS development through detailed hardware and software development in the RAON accelerator and explain the future plans.

INTRODUCTION

The RAON accelerator [1] produces various kinds of beams from proton to uranium to accelerate and transport to the target in the experimental hall. These beams can be accelerated to an energy of about 200 MeV/u, with a power of up to 400 kW. Various devices such as ion sources, magnets, superconducting cavities, etc. are installed to generate and accelerate beams, and sudden interlocks in the devices lead to the beam loss during operation. This beam loss can cause significant damage to the device, and therefore a machine protection system (MPS) is required to minimize such damage in the RAON accelerator. Currently, we are developing the MPS into four parts for efficient operation: a fast protection system (FPS), a slow interlock system (SIS), a post-mortem system (PMS), and a run permit system (RPS). First, the FPS is fabricated on an field programmable gate array (FPGA) basis and collects interlock signals from the beam loss monitor (BLM), beam current monitor (BCM), low-level radio-frequency (LLRF) system, etc. within a few tens of microseconds and sends the beam stop signal to the mitigation devices like a chopper, RFQ LLRF, and so on. Secondly, the SIS is fabricated on programmable logic controller (PLC) basis and collects interlock signals from devices such as cryogenics, vacuum, etc., and transmits interlock information to the FPS within a few tens of milliseconds. Thirdly, the PMS is a system for storing and analyzing information of interlock signals to prevent future accidents. At last, the RPS is a system for determining beam operation status by checking the state of accelerator devices corresponding to a machine mode and a beam mode before operation. Figure 1 shows the configuration of the RAON MPS.

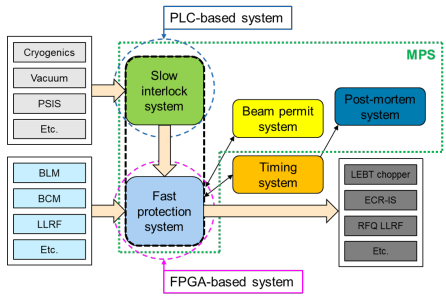

Figure 1: Layout of the RAON machine protection system. The machine protection system consists of the fast protection system, the slow interlock system, the post-mortem system, and the run permit system.

FAST PROTECTION SYSTEM

The RAON FPS consists of a mitigation node acting as a master and an acquisition node acting as a slave. This FPS consists of two mitigation nodes including a back-up and dozens of acquisition nodes as shown in Fig. 2. The prototype of the FPS was developed in 2016 and successfully tested at the RISP test facility. The test results of the prototype were presented at ICABU2017 workshop [2]. Based on these results, The FPS product, including one mitigation node and seven acquisition nodes, is currently under development [3] and will be finished at the end of 2018.

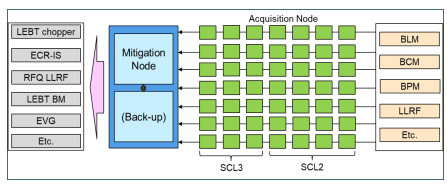

Figure 2: Layout of the fast protection system which has mitigation nodes and acquisition nodes. The acquisition node collects the interlock signals, and the mitigation node sends signals to mitigation devices.

The Mitigation node is manufactured using Xilinx Zynq ultrascale+ XCZU9EG chip. In this node, eight SFP+ transceivers are installed for optical communication, and 24 sub-miniature version A (SMA) ports are located on the back panel for signal transmission with mitigation devices. The printed circuit board (PCB) of the mitigation node is now being manufactured, and the test is in progress. Figure 3 shows the wiring diagram of the mitigation node. The

* hcjin@ibs.re.kr

main board where the Zynq chip is located is connected to the daughter board which sends the output signal, and power is supplied through the switched-mode power supply (SMPS). Unlike mitigation node, the acquisition is manufactured using Xilinx Zynq XC7Z100 chip, and the wiring diagram of the acquisition node is shown in Fig. 4 and the electric power is supplied through SMPS with lower power than mitigation node. Sixty-four interlock signals collected through the daughter board are sent to the main board.

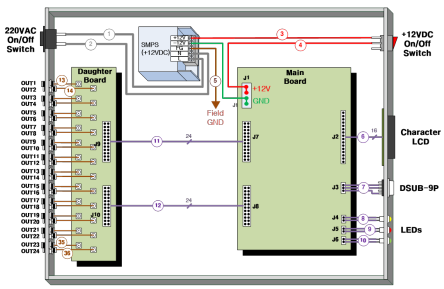

Figure 3: The connection diagram of the mitigation node.

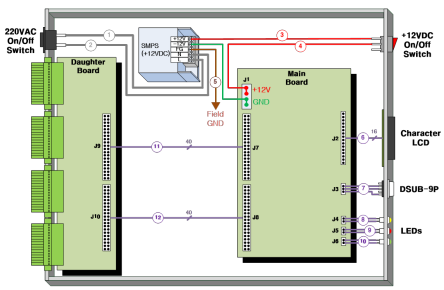

Figure 4: The connection diagram of the acquisition node.

SLOW INTERLOCK SYSTEM

RAON SIS collects interlock signals from the PLC controlled devices such as cryogenics, vacuum, etc. and then transmits the information to the acquisition node of the FPS. The SIS prototype was also developed in 2016, and the performance verification was successfully completed at the RISP test facility [2]. Based on the prototype results, the SIS production is currently in progress. The configuration of the SIS is shown in Fig. 5. The SIS PLC in a control rack consists of a CPU for signal processing, a module for 16 digital outputs, and modules for 144 digital inputs. The bit processing time of the CPU is less than 48 nanoseconds. In addition, a signal relay, a circuit protector, and a SMPS are located below the SIS PLC. These SIS sets will be located in 23 control racks for low energy superconducting linac section and collect nearby local interlock signals.

POST-MORTEM SYSTEM

The development of the PMS is in progress with the development of the FPS, and the signal processing of the PMS is as shown in Fig. 6. When the interlock signal is collected at the acquisition node, the signal is transmitted from the

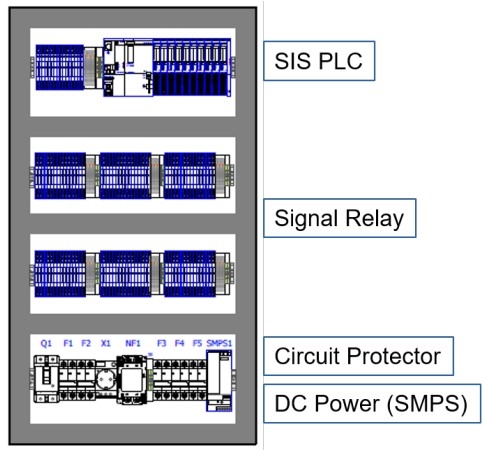

Figure 5: Layout of the slow interlock system in the control lack. It consists of a SIS PLC, a signal relay, a circuit protector, and a DC power.

mitigation node to the event generator (EVG) of the timing system. After that, when the signal is transmitted from the EVG to the acquisition nodes, the interlock data is saved at the acquisition node memory for ±200 milliseconds in a unit of 1 microsecond. The stored information can then be verified at the CS-Studio (CSS) operator interface (OPI) through the EPICS IOC. To develop and verify this PMS, we are testing using FPS hardware under development, and the block diagram in this test is shown in Fig. 7. The CSS screen of the PMS is shown in Fig. 8.

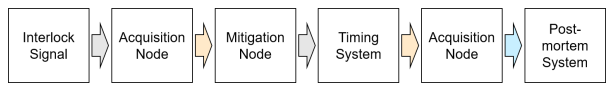

Figure 6: Signal flow of the post-mortem system. The PMS data is saved at an acquisition node memory and sent to the data server through the EPICS IOC.

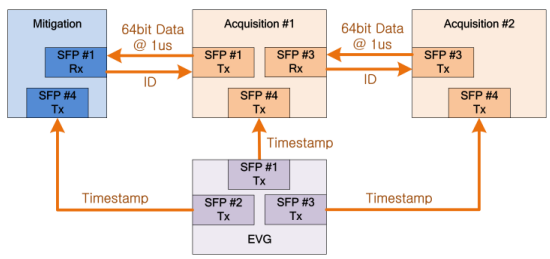

Figure 7: Block diagram of the post-mortem system test.

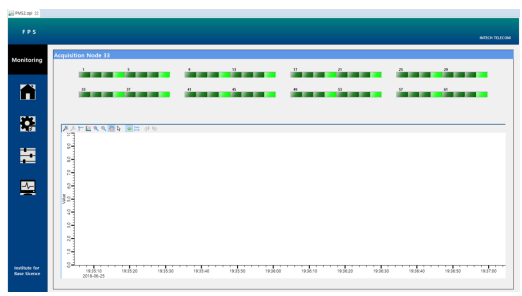

Figure 8: CSS screen of the post-mortem system.

RUN PERMIT SYSTEM

The RAON accelerator has various operating modes because various types of beams are used for experimental purposes. Therefore, for efficient operation, the accelerator operation mode is divided into a machine mode for determining the devices to be used and a beam mode for determining the type and state of the beam. Tables 1 and 2 show examples of machine mode and beam mode in the RAON accelerator, respectively. More accurate information will be determined as commissioning proceeds with the beam physics group. Figure 9 shows the CSS test screen of the current RPS. This RPS operates with standby, run, fault, and stop states. Since 2019, The accelerator equipment will be installed in accelerator tunnels, and the RPS upgrade will be continued.

Table 1: Machine Mode Example

Mode	Description	Remark
MM0	Maintenance	No beam
MM1	LEBT tuning	Ion source, RFQ
MM2	MEBT tuning	Rebuncher
MM3	Linac tuning	SCL3, SCL2
MM4	P2DT tuning	Buncher, charge stripper
MM5	Secondary beam test	Target
MM6	User operation	Target

Table 2: Beam Mode Example

Mode	Description	Remark
BM0	Maintenance	No beam
BM1	Pulse mode	Time structure, beam intensity
BM2	CW mode	Normal operation, beam power

SUMMARY

We have presented the current development status of the RAON MPS which includes the FPS, the SIS, the PMS, and the RPS. Based on the prototype results of the FPS, the FPS product is under development using Zynq chips, and it will be finished at the end of 2018. The FPS collects the interlock signals from BLM, BCM, LLRF, etc. and sends a beam stop signals to the mitigation devices within a few tens of microseconds. The SIS product is also being manufactured using a PLC and will collect the interlock signals from the PLC controlled devices. The development of the PMS is proceeding with the FPS development, and a data saving testing is in progress. For the efficient accelerator operation, the RPS is also being developed with the machine mode and the beam mode, and the upgrade of the RPS will be continued with the installation of the accelerator equipment after 2019.

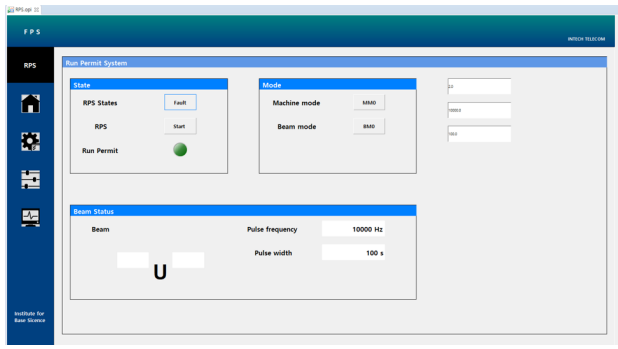

Figure 9: CSS test screen of the run permit system.

ACKNOWLEDGEMENTS

This work was supported by the Rare Isotope Science Project of Institute for Basic Science funded by Ministry of Science, ICT and Future Planning and National Research Foundation of Korea (2013M7A1A1075764).

REFERENCES

[1] D. Jeon *et al.*, "Design of the RAON accelerator systems", *Journal of the Korean Physical Society* 65.7 (2014).

[2] ICABU2017, `https://indico.cern.ch/event/647155/`

[3] H. Jin *et al.*, "Progress and plan of the fast protection system in the RAON accelerator", *in Proc. HB'18*, Daejeon, Korea, June 2018. `doi:10.18429/JACoW-HB2018-WEP2PO015`